CLAIMS

1-26. (canceled)

27. (currently amended) In a system comprising a first processor and one or more other processors, a method for applying one or more interrupt signals to the one or more other processors, the method comprising:

(a) generating, in the first processor, a data signal having one or more data bits, wherein each data bit has either a first bit value or a second bit value;

(b) transmitting the data signal from a data port of the first processor to a signal unit external to the first processor and the one or more other processors;

(c) converting, in the signal unit, the data signal into one or more interrupt signals by analyzing the bit value of each of one or more data bits in the data signal, wherein each analyzed data bit in the data signal having a specified bit value corresponds to a different interrupt signal; and

(d) transmitting each interrupt signal from the signal unit to an interrupt port of an other processor.

28. (currently amended) The invention of claim 27, wherein:

the data signal has a plurality of analyzed data bits having the specified value;

the signal unit converts the data signal into a plurality of interrupt signals; and

each interrupt signal is transmitted to a different interrupt port of an other processor.

29. (previously presented) The invention of claim 28, wherein at least two interrupt signals are transmitted to two different interrupt ports of a single other processor.

30. (previously presented) The invention of claim 28, wherein at least two interrupt signals are transmitted to interrupt ports of at least two different other processors.

31. (currently amended) The invention of claim 27, wherein the signal unit detects a transition in each analyzed data bit of the data signal over time to determine when to generate a corresponding interrupt signal.

32. (previously presented) The invention of claim 31, wherein the signal unit detects the transition by:

storing sequential values for the corresponding data bit in two registers; and

comparing outputs from the two registers to detect a difference between the two sequential values.

33. (previously presented) The invention of claim 32, wherein:

the first processor transmits an address signal to the signal unit; and

the signal unit compares the address signal to a specified value to determine whether to store the two sequential values in the two registers.

34. (previously presented) The invention of claim 27, wherein each interrupt signal is transmitted from the signal unit to a corresponding interrupt port of a corresponding other processor via a dedicated line.

35. (previously presented) The invention of claim 34, wherein the data signal is transmitted from the first processor to the signal unit via a shared data bus.

36. (currently amended) The invention of claim 27, further comprising applying an interrupt signal from an other processor to the first processor by:

(1) generating, in the other processor, an other data signal having one or more other data bits, wherein each other data bit has either the first bit value or the second bit value;

(2) transmitting the other data signal from a data port of the other processor to an other signal unit external to the first processor and the one or more other processors;

(3) converting, in the other signal unit, the other data signal into one or more other interrupt signals by analyzing the bit value of each of one or more other data bits in the other data signal, wherein each analyzed other data bit in the other data signal having the specified bit value corresponds to a different other interrupt signal; and

(4) transmitting an other interrupt signal from the other signal unit to an interrupt port of the first processor.

37. (previously presented) The invention of claim 36, wherein at least one other interrupt signal is transmitted from the other signal unit to an interrupt port of at least one other processor.

38. (currently amended) A system comprising a first processor connected to one or more other processors via a signal unit external to the first processor and the one or more other processors, wherein:

the first processor is adapted to (i) generate a data signal having one or more data bits, wherein each data bit has either a first bit value or a second bit value, and (ii) transmit the data signal from a data port of the first processor to the signal unit; and

the signal unit is adapted to (i) convert the data signal into one or more interrupt signals by analyzing the bit value of each of one or more data bits in the data signal, wherein each analyzed data bit in the data signal having a specified bit value corresponds to a different interrupt signal, and (ii) transmit each interrupt signal from the signal unit to an interrupt port of an other processor.

39. (currently amended) The invention of claim 38, wherein:

the data signal has a plurality of analyzed data bits having the specified value;

the signal unit is adapted to convert the data signal into a plurality of interrupt signals; and

the signal unit is connected to transmit each interrupt signal to a different interrupt port of an other processor.

40. (previously presented) The invention of claim 39, wherein the signal unit is connected to transmit at least two interrupt signals to two different interrupt ports of a single other processor.

41. (previously presented) The invention of claim 39, wherein the signal unit is connected to transmit at least two interrupt signals to interrupt ports of at least two different other processors.

42. (currently amended) The invention of claim 38, wherein the signal unit is adapted to detect a transition in each analyzed data bit of the data signal over time to determine when to generate a corresponding interrupt signal.

43. (currently amended) The invention of claim 42, wherein the signal unit comprises:

two registers adapted to store sequential values for each analyzed data bit; and

logic adapted to compare outputs from the two registers to detect the transition for a corresponding data bit as a difference between the two sequential values.

44. (previously presented) The invention of claim 43, wherein:

the first processor is adapted to transmit an address signal to the signal unit; and

the signal unit comprises an address decoder adapted to compare the address signal to a specified value to determine whether to store the two sequential values in the two registers.

45. (previously presented) The invention of claim 38, wherein the signal unit is connected to transmit each interrupt signal to a corresponding interrupt port of a corresponding other processor via a dedicated line.

46. (previously presented) The invention of claim 45, wherein the first processor is connected to transmit the data signal to the signal unit via a shared data bus.

47. (currently amended) The invention of claim 38, further comprising an other signal unit connecting an other processor to the first processor, wherein:

the other signal unit is external to the first processor and the one or more other processors;

the other processor is adapted to (i) generate an other data signal having one or more other data bits, wherein each other data bit has either the first bit value or the second bit value, and (ii) transmit the other data signal from a data port of the other processor to the other signal unit; and

the other signal unit is adapted to (i) convert the other data signal into one or more other interrupt signals by analyzing the bit value of each of one or more other data bits in the other data signal, wherein each analyzed other data bit in the other data signal having the specified bit value corresponds to a different other interrupt signal and (ii) transmit an other interrupt signal from the other signal unit to an interrupt port of the first processor.

48. (previously presented) The invention of claim 47, the other signal unit is adapted to transmit at least one other interrupt signal to an interrupt port of at least one other processor.

49. (currently amended) A first processor for a system comprising the first processor connected to one or more other processors via a signal unit external to the first processor and the one or more other processors, wherein:

the first processor is adapted to (i) generate a data signal having one or more data bits, wherein each data bit has either a first bit value or a second bit value, and (ii) transmit the data signal from a data port of the first processor to the signal unit; and

the signal unit is adapted to (i) convert the data signal into one or more interrupt signals by analyzing the bit value of each of one or more data bits in the data signal, wherein each analyzed data bit in the data signal having a specified bit value corresponds to a different interrupt signal, and (ii) transmit each interrupt signal from the signal unit to an interrupt port of an other processor.

50. (previously presented) The invention of claim 49, wherein the first processor is adapted to transmit the data signal to the signal unit via a shared data bus.

51. (currently amended) A signal unit for a system comprising a first processor connected to one or more other processors via the signal unit external to the first processor and the one or more other processors, wherein:

the first processor is adapted to (i) generate a data signal having one or more data bits, wherein each data bit has either a first bit value or a second bit value, and (ii) transmit the data signal from a data port of the first processor to the signal unit; and

the signal unit is adapted to (i) convert the data signal into one or more interrupt signals by analyzing the bit value of each of one or more data bits in the data signal, wherein each analyzed data bit in the data signal having a specified bit value corresponds to a different interrupt signal, and (ii) transmit each interrupt signal from the signal unit to an interrupt port of an other processor.

52. (currently amended) The invention of claim 51, wherein:

the data signal has a plurality of analyzed data bits;

the signal unit is adapted to convert the data signal into a plurality of interrupt signals; and

the signal unit is adapted to transmit each interrupt signal to a different interrupt port of an other processor;

the signal unit is adapted to transmit at least two interrupt signals to two different interrupt ports of a single other processor;

the signal unit is adapted to transmit at least two interrupt signals to interrupt ports of at least two different other processors;

the signal unit is adapted to detect a transition in each analyzed data bit of the data signal over time to determine when to generate a corresponding interrupt signal;

the signal unit is adapted to receive the data signal from the first processor via a shared data bus; and

the signal unit is adapted to transmit each interrupt signal to a corresponding interrupt port of a corresponding other processor via a dedicated line.